A New Circuit Structure for Microwave Frequency Doublers

Josef Fikart and Yongnan Xuan

MPR Teltech Ltd.
8999 Nelson Way, Burnaby, Canada

Abstract

A new circuit structure for microwave frequency doublers is presented, which features effective suppression of fundamental and odd harmonics (> 50 dB), conversion gain (> 3dB) and simplicity of the circuit. Furthermore, it can be used in both balanced and unbalanced output configurations, without requiring baluns or transformers. Experimental results are also given in the paper.

I. Introduction

Frequency doublers are widely used in microwave subsystem as part of multiplier chains or for other purposes. Typically, frequency doubling is realized by feeding the signal through nonlinear devices, such as diodes or transistors, and then extracting the second harmonic and rejecting other frequency components. The basic problem in designing a doubler is that of achieving sufficient suppression of undesired signals at the output port. Circuit components such as microstrip quarter-wavelength or radial open stubs can be used in the output port of the doublers [1,2], which shunt the fundamental frequency component to ground to prevent it from appearing at the output. Similar techniques may also be used at the input port to short-circuit the second harmonic to ground to achieve good input-output port isolation. Rejection of the unwanted harmonics over a wider bandwidth can be achieved using balanced configurations as those described in [3] and [4], since the fundamental and odd harmonics are inherently suppressed in the circuits. A drawback associated with these structures is the requirement for baluns, which increase the loss, physical dimensions and complexity of the circuits.

A new circuit structure has been developed for microwave frequency doublers. It features effective suppression of fundamental and odd harmonics, conversion gain and simplicity of the circuit. Furthermore, either balanced or unbalanced configuration can be selected at the output without requiring baluns or transformers, thereby reducing the loss and simplifying the circuit. Nonlinear computer simulation was carried out during the design of a MMIC doubler using the present circuit configuration. Very good performance of the circuit was predicted and then verified by experimental results.

CH3277-1/93/0000-0407$01.00 © 1993 IEEE

In the following, the proposed circuit structure is illustrated, together with the description on the principle of its operation, design conside- rations and measured results.

II. The Doubler Circuit and Its Operation

The doubler circuit is shown in Fig.1. It consists of a diode bridge functioning as a full-wave rectifier, a differential amplifier using a pair of transistors, and three simple LC circuits for DC decoupling and matching, used at the input, the output, and between the rectifier and the amplifier.

The input signal at frequency f is applied to node 1 of the circuit and is full-wave rectified by the diode bridge. The two outputs from the rectifier at nodes A and B are applied to the differential amplifier, which in turn also supplies two outputs. These can be then used in either balanced or unbalanced configuration.

Both odd and even order harmonics are generated by the full-wave rectification. The odd and even harmonics have different relative phase relationships at the output nodes of the rectifier. The fundamental component and all odd harmonics at nodes A and B are in common mode (in phase), with equal amplitudes when the circuit is symmetric which in practice can well be realized using MIC and MMIC technologies. These harmonic components are effectively suppressed by the amplifier because of the well known common mode rejection characteristics of differential amplifiers. Further suppression is achieved if the two outputs of the amplifier are used in a balanced configuration; however because of the above mentioned common mode rejection, the suppression performan- ce of the circuit even when using the outputs in an unbalanced mode is quite satisfactory. This is one of the desirable features of the present frequency doubler circuit structure.

In contrast to the odd harmonics, the even harmonics at the output of the rectifier are in a differential mode (out of phase). The desired second harmonic is generated at a relatively strong level by the full-wave rectification and is then further amplified by the differential amplifier. Although other even harmonics (4th, 6th,...) are in a differential mode, their levels are lower than that of the second harmonic. In addition, and more importantly, they are sufficiently removed from the second harmonic so that they can be relatively easily filtered out by the frequency response of the circuit. A balanced output signal can be obtained between the two output nodes (2 and 3) of the doubler. Otherwise, if unbalanced output signals are desired, they can be obtained directly at the two output nodes.

It can be seen from the above discussion that there are a number of advantages in using the full-wave rectifier - differential amplifier combination for frequency doubling. For a given CW signal, full-wave rectification generates relatively high level of second harmonic content. The use of the diode bridge as the rectifier also implements the unbalanced-to-balanced transformation, which eliminates the need

for baluns or transformers and the associated power transmission loss in the input circuit. As for the differential amplifier, its properties of rejecting common mode input signals and amplifying differential mode signals are desirable and are fully utilized for the present application. It is especially advantageous that the suppression of the unwanted fundamental and odd harmonics is realized by mode rejection, instead of frequency filtering, which allows the doubler circuit to operate over a wider bandwidth with satisfactory performance.

DC bias applied to the diode bridge is optional to achieve optimum performance of the rectifier for different input power levels. For lower levels of input signals, it is useful to bias the diodes to operate at a point close to the knee of their I-V curves. However, for higher input power levels, biasing will not significantly contribute to conversion efficiency. The transistors in the differential amplifier should be biased for operation in their linear amplification regions. This is required for the second harmonic to be amplified without further generation of its harmonics, and for maintaining the electrical symmetry of the circuit. Otherwise, the performance, in particular the common mode rejection ratio (CMRR), of the differential amplifier will deteriorate.

III. Experimental Results

Using the above described circuit structure, a MMIC frequency doubler has been designed and fabricated using the Texas Instruments MMIC foundry. The layout of the circuit is shown in Fig.2, where the two key blocks - the full-wave rectifier and the differential amplifier - are indicated. Bias circuits for both the rectifier and the amplifier are included within the chip. Special attention has been paid to keep the symmetry of the physical layout, although computer simulation showed that the circuit would work satisfactory with up to ten percent of dimensional tolerance in fabrication. The doubler was intended to be used with an input power level of 6 dBm at about 7.8 GHz. It has been successfully tested with consistent results. The fundamental frequency suppression was found to be over 50 dB, while better than 3 dB conversion gain was achieved. This can be seen in Fig.3 where the frequency response of gain and of fundamental suppression is shown. The dependence of these parameters on the input power level is given in Fig.4.

IV. Conclusion

A new circuit structure for microwave frequency doublers has been presented. It has been used in the design of a MMIC doubler. Its major advantages are effective suppression of the unwanted odd-order harmonics and conversion gain to the desired second harmonic. They have been demonstrated by computer simulation and further verified by measured results for the MMIC circuit. Furthermore, the circuit requires no baluns or transformers and both a balanced or unbalanced output is available.

Acknowledgment

The authors would like to acknowledge the co-operation of their colleagues and thank Dr. W. Bosch, now at M/A Com, for his advice during the development of the circuit.

References

[1] C. Rauscher, "High-Frequency Doubler Operation of GaAs Field-Effect Transistors", IEEE Trans. Microwave Technology and Techniques, Vol.31, No.6, June 1983, pp462-473

[2] P.D. Chow, et al, "A 44 GHz HEMT Doubler/Amplifier Chain"' IEEE Int. Symp. on Microwave Technology and Techniques, 1990, pp603-606

[3] R. Gilmore, "Concepts in the Design of Frequency Multipliers", Microwave Journal, March 1987, pp129-139

[4] I. Angelov, et al, "A Balanced Millimeter Wave Doubler Based on presudomorphic HEMTs" , IEEE Int. Symp. on Microwave Technology and Techniques, 1992, pp353-356

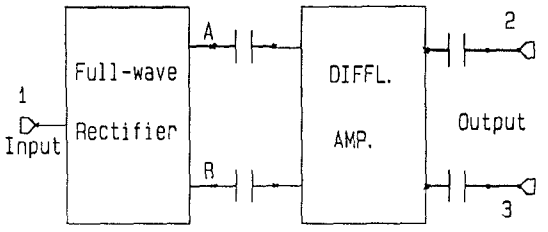

Fig. 1 Block Diagram of Freq. Doubler

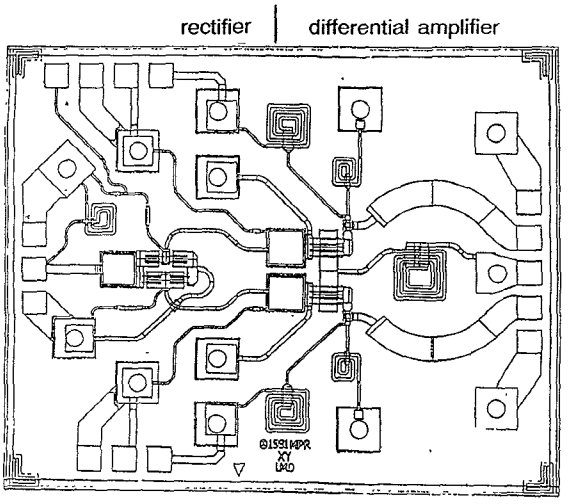

Fig.2 Layout of MMIC Frequency Doubler

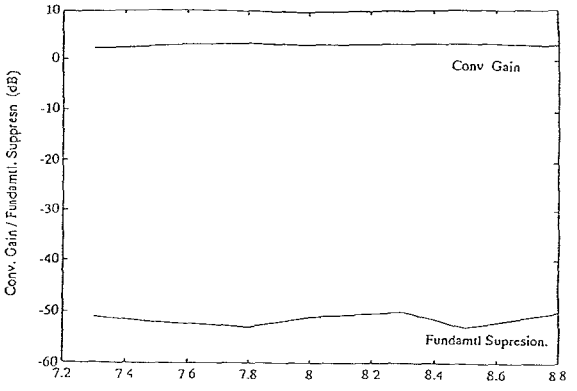

Fig.3 Measured Conv. Gain and Fundamtl. Supresion. VS Freq (GHz)

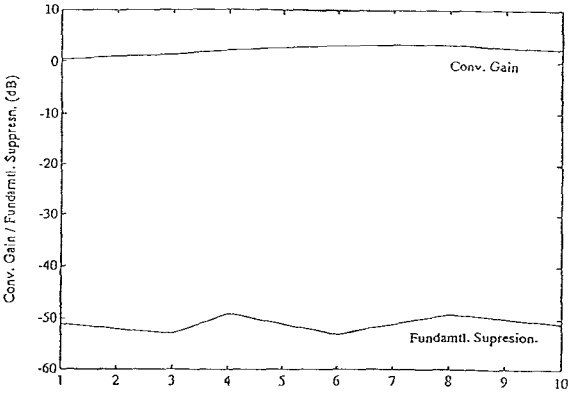

Fig 4 Measured Conv Gain and Fundamtl Supresion VS Pin (dBm)